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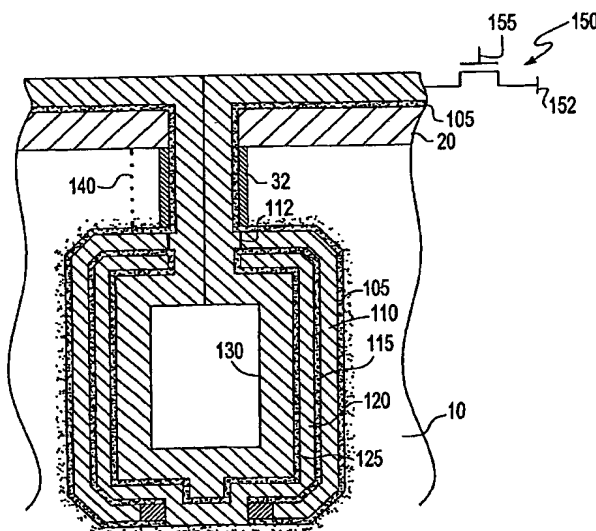
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(54) Title: **FOLDED NODE TRENCH CAPACITOR**



(57) **Abstract:** A trench capacitor (60) is filled with a set of two or more storage plates (110, 120, 130) by consecutively depositing layers of dielectric (105, 115, 125) and conductor (110, 120, 130) and making contact to (16) the ground plates by etching an aperture through the plates to the buried plate (15) in the substrate (10) and connecting the one or more ground plate (120) to the substrate (10); the charge storage plates (120, 130) are connected at the top of the capacitor by blocking the end of the first plate (112) during the formation of the second ground plate (120) and exposing the material of the first storage plate (110) during deposition of the second storage plate (130).



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

1
2
3 Folded Node Trench Capacitor
4
5

6 TECHNICAL FIELD
7

8 The field of the invention is that of forming integrated circuit trench capacitors, in
9 particular capacitors for use in DRAM cells.
10

11
12 BACKGROUND OF THE INVENTION
13

14 Semiconductor memory devices, and particularly Dynamic Random Access Memory
15 (DRAM) devices are well known. An essential feature of a DRAM is a memory cell. A
16 cell comprises a capacitor for storing charge and an access transistor (also referred to as a
17 pass transistor or a pass gate) for transferring charge to and from the capacitor. Trench, or
18 deep trench (DT), capacitors are typical and are well known. A cell also comprises a
19 means (often referred to as a strap) for connecting one transistor source/drain region to
20 the capacitor. At the present state of the art, more than 256 million DRAM cells are
21 present on a memory chip, organized in the form of an array. Thus, because cell size
22 determines chip density, size and cost, reducing cell area is the DRAM designer's primary
23 goal. Cell area may be reduced by shrinking the individual feature size, or by forming
24 structures which make more efficient use of the chip surface area. The latter approach is

1 particularly desirable.

2

3 In a typical process for fabricating DRAM devices having trench capacitors, the capacitor
4 structure is completely formed prior to the formation of the transistor gate conductor
5 (GC) structure. Thus, a typical process sequence involves the steps of opening the trench,
6 filling the trench, forming the node conductors, then forming the gate stack structure.

7

8 As is known in the art, integrated circuits (ICs) or chips employ capacitors for charge
9 storage purposes. An example of an IC that employs capacitors for storing charge is a
10 memory IC, such as a dynamic random access memory (DRAM) chip. The level of the
11 charge ("0" or "1") in the capacitor represents a bit of data.

12

13 A DRAM chip includes an array of memory cells interconnected by rows and columns.
14 Typically, the row and column connections are referred to as wordlines and bitlines,
15 respectively. Reading data from or writing data to the memory cells is accomplished by
16 activating the appropriate wordlines and bitlines.

17

18 Typically, a DRAM memory cell comprises a transistor connected to a capacitor. The
19 transistor includes two diffusion regions separated by a channel, opposite which is located
20 a gate. Depending on the direction of current flow between the diffusion region, one is
21 referred to as the drain and the other the source. The terms "drain" and "source" are herein
22 used interchangeably to refer to the diffusion regions. The gate is coupled to a wordline
23 and one of the diffusion regions is coupled to a bitline. The other diffusion region is
24 coupled to the capacitor. Applying an appropriate voltage to the gate switches the

1 transistor on, enabling current to flow through channel between the diffusion regions to
2 form a connection between the capacitor and bitline. Switching off the transistor severs
3 this connection by preventing current flowing through the channel.

4
5 The charge stored in the capacitor dissipates over time due to current leakage therefrom.
6 Before the charge dissipates to an indeterminate level (below a threshold), the node has to
7 be refreshed.

8
9 Continued demand to shrink devices has facilitated the design of DRAMs having greater
10 density and smaller feature size and cell area. To produce cells that occupy less surface
11 area, smaller components such as capacitors are used. However, the use of smaller
12 capacitors results in decreased storage capacity, which can adversely affect the
13 performance and operability of the memory device. For example, sense amplifiers require
14 an adequate signal level to reliably sense the information in the cells. The ratio of storage
15 capacitance to bitline capacitance is crucial in determining the signal level. If the
16 capacitor becomes too small, this ratio may be too small to provide an adequate signal.
17 Also, smaller storage capacity requires higher refresh frequency.

18
19 One type of capacitor that is commonly employed in DRAMs is a trench capacitor. A
20 trench capacitor is a three-dimensional structure formed in the silicon substrate.
21 Increasing the volume or capacitance of the trench capacitor can be achieved by etching
22 deeper into the substrate. As such, increasing the capacitance of the trench capacitor does
23 not increase the surface area of the cell.

24

1 A conventional trench capacitor comprises a trench etched into the substrate. The trench
2 is typically filled with n+ doped poly which serves as an electrode of the capacitor
3 (referred to as the storage node). Optionally, a second electrode of the capacitor, referred
4 to as a "buried plate," is formed by out-diffusing n+ dopants from a dopant source into a
5 region of the substrate surrounding the lower portion of the trench. A n+ doped silicate
6 glass such as Arsenic doped silicate glass (ASG) serves as the dopant source. A node
7 dielectric comprising nitride is provided to separate the two electrodes of the capacitor.

8
9 In the upper portion of the trench, a dielectric collar is provided to prevent leakage from
10 the node junction to the buried plate. The node dielectric in the upper portion of the
11 trench where the collar is to be formed is removed prior to its formation. Removal of the
12 nitride prevents vertical leakage along the collar.

13
14 There is constant pressure to reduce the dimensions of DRAM cells and constant pressure
15 to save cost by reducing the depth of the trench.

16 Planar capacitors use two or more capacitor storage plates in the same silicon area.

17

18 Trench capacitor technology has not been able to place two or more storage plates in a
19 trench.

20

21

22 SUMMARY OF THE INVENTION

23

24 The invention relates to a trench capacitor having two or more plates within the trench to

1 increase the surface area of the capacitor.

2

3 A feature of the invention is successive deposition of a first variable capacitor plate, a
4 ground plate and a second variable capacitor plate.

5

6 Another feature of the invention is etching through the bottom of a stack of plates to
7 make contact with the substrate and closing off edges of conductive layers by forming
8 dielectric on the exposed edges.

9

10

11 BRIEF DESCRIPTION OF THE DRAWINGS

12

13 Figure 1 shows a silicon substrate containing a deep trench after the "bottle etch" step.

14

15 Figure 2 shows the same area after forming the buried plate by gas phase doping.

16

17 Figure 3 shows the area after depositing the first conductive layer.

18

19 Figure 4 shows the area after depositing the second dielectric layer.

20

21 Figure 5 shows the area after etching through the previous layers to make contact with the
22 buried plate.

23

24 Figure 6 shows the area after closing off exposed conductors.

1

2 Figure 7 shows the area after clearing the upper portion of the trench after the deposition
3 of the second conductive layer.

4

5 Figure 8 shows the area after forming the third dielectric layer.

6

7 Figure 9 shows the area after exposing the edge of the first capacitor plate in preparation
8 for the second capacitor plate.

9

10 Figure 10 shows the structure after the deposition of the second capacitor plate.

11

12

13 DETAILED DESCRIPTION

14

15 The inventive process begins with conventional steps of etching a deep trench that will
16 hold the capacitor. Illustratively, the deep trench etch is performed with a TEL SCCM
17 etch tool and NF₃/HBr chemistry.

18

19 In current practice, the trenches used for DRAM cells are etched to a depth of about eight
20 microns. It is an advantageous feature of the invention that the increased capacitance
21 provided by the inventive process can be used to provide a trench that is less deep and
22 therefore reduce the cost of the integrated circuit.

23

24 Figure 1 shows the structure after steps of depositing a protective liner on the trench

1 walls, stripping the liner in the lower portion and etching the bulk silicon substrate
2 laterally in a wet etch or isotropic dry etch.

3
4 Those skilled in the art will appreciate that the direction of etching may be controlled
5 over a wide range - from the highly directional process used to etch the initial trench to an
6 isotropic process having a substantial lateral etching action.

7
8 In this example, the initial trench width of nominally 100nm is expanded to a nominal
9 250nm by the bottle etch, producing aperture 60 in a capacitor area denoted generally by
10 numeral 50. Particular examples of the invention will have variable dimensions
11 depending on the cell layout and the ground rules for the particular process being used.

12
13 Illustratively, the protective liner 32 is formed of 2nm oxide, 4nm nitride, 10nm poly and
14 6nm of nitride. Other combinations of materials and thicknesses may be used for
15 particular needs.

16
17 At the top of the Figure, pad nitride 20 protects the surface of substrate 10 and bracket 30
18 indicates a recess depth that defines the depth of the capacitor portion and also defines the
19 upper portion where the vertical transistor of the DRAM cell will be formed.

20
21 The process followed is that, after liner 32 is formed, resist is formed in the trench and
22 recessed to a nominal depth of 1.5 microns, referred to as the capacitor top position. The
23 outer nitride layer of liner 32 is stripped, exposing the poly layer beneath. The remaining
24 resist in the lower portion of the trench is stripped, to avoid exposing it to the high

1 temperature of the oxidation step. The poly in the upper portion is then is oxidized, so
2 that liner 32 has an outer layer of oxide in the upper portion and an outer layer of nitride
3 in the lower portion.

4
5 Layer 32 is then stripped in the lower portion. The outer nitride is stripped while the
6 oxide in the upper portion protects the walls there. Similarly, the oxide in the upper
7 portion protects it while the poly and the second nitride layer in the lower portion are
8 removed. When the last layer (oxide) in the lower portion is removed, the oxide in the
9 upper portion will be attacked. If the oxide in the upper portion is thick enough, it will
10 remain. If not, the poly or the nitride below it will protect the surface of silicon 10. The
11 result is shown in Figure 1.

12
13 Optionally, a layer of hemispherical grained silicon (HSG) may be put down in a
14 conventional process to improve the surface area.

15
16 Figure 2 shows the result of gas phase doping with arsenic in the lower portion to form
17 buried plate 15 that will be the ground plate (capacitor plate) of the capacitor and the
18 deposition of a conformal nitride liner 105, illustratively 4 nm thick, that extends
19 throughout the lower portion and also over the upper portion of the trench and the top of
20 pad nitride 20. Dielectric 105 may optionally be subjected to a "re-ox" procedure in
21 which the node nitride is exposed to an oxidizing ambient. This process improves the
22 electrical properties of the nitride, i.e. it reduces the leakage current through the node
23 nitride when a voltage is applied.

24

1 Figure 2 shows the result of depositing a conformal layer of doped poly 110 that will
2 form the first storage plate of the capacitor, illustratively 30 nm thick, that also covers the
3 lower portion and also the narrower upper portion and the top of the substrate. This
4 shows the basic structure of the capacitor process - a layer of dielectric followed by a
5 layer of conductor. The challenge in making a multi-plate capacitor is to connect the
6 various ground plates and storage plates reliably.

7
8 Figure 4 shows the result of depositing a second nitride layer 115, having the same
9 thickness as layer 105. Figure 4 shows a narrow gap in the upper portion between the
10 poly layers on the two sides. This gap would plug up the narrow portion and prevent
11 deposition of further layers if it is not cleared.

12 Figure 5 shows the result of etching layers 115 and 110 with a directional dry etch. At the
13 bottom of the Figure, a bottom aperture with a surface 16 indicates the exposed surface of
14 the bulk silicon that has been doped to form buried plate 15. This area will provide the
15 electrical contact between the buried plate and the interior ground plate of the multi-plate
16 capacitor. Surfaces 112 are the exposed ends of layer 110. These surfaces must be
17 isolated from the ground plate that will be put down in order to avoid shorting the
18 capacitor plates.

19
20 Figure 6 shows the result of a thermal oxidation step that forms an oxide plug 122,
21 nominally 30 nm thick, on upper and lower exposed surfaces 112 of poly 110. There will
22 be some oxide grown on surface 16 that can be removed by a short wet etch or directional
23 dry etch to maintain a good contact on surface 16.

1 A second ground (capacitor) plate 120 is formed by depositing a conformal layer of
2 doped poly with the same parameters as used for layer 110. At the bottom of the Figure,
3 electrical contact has been made between ground plate 120 and buried plate 15. Aperture
4 60 is filled again with resist 132 that is non-critically recessed past the narrow portion of
5 the trench. Another poly cleanup is performed to remove the poly 120 from the upper
6 portion of the trench, as far down as the top of layer 120. The result is shown in Figure 7.
7 Resist 132 is then stripped, exposing the surface of poly 120.
8
9 Figure 8 shows the result of nitriding the surface of poly 120 to produce nitride layer 125,
10 illustratively the same thickness as layers 105 and 115. This is a thermal nitride process,
11 not a conformal deposition, so that nitride does not form on the surface of oxide plugs
12 122 or on layer 105 in the narrow portion of the trench.
13
14 Bracket 62 indicates the width of the upper trench. It can be seen that the upper contact
15 position of plate 110 is outside the area of the upper trench and there is no straight line
16 reaching from the surface of substrate 10 to the contact edge of plate 110.
17 Figure 9 shows the result of a wet etch that removes oxide plugs 122 at the upper portion
18 of the capacitor without attacking nitride 125 or nitride 105 in the upper portion. A clean
19 surface 123 on poly 110 is now available to make contact with the second poly storage
20 plate.
21
22 Figure 10 shows the result of the conformal deposition of poly 130, which forms the
23 second storage plate of the capacitor. The capacitor structure is buried ground plate 15,
24 first dielectric 105, first storage plate 110, second dielectric 115, second ground plate 120,

1 third dielectric 125 and second storage plate 130.

2

3 At the top of the Figure, dotted line 140 denotes schematically the location of a vertical
4 transistor that completes the DRAM cell. The fabrication of the vertical transistor is well
5 known in the art.

6

7 At the upper right of the Figure, a transistor symbol 150, with bitline 152 and wordline
8 150 denotes the electrical completion of the DRAM cell and its connection to the lines of
9 a memory array.

10

11 A trench capacitor according to the invention may be used with vertical or planar
12 transistors in a DRAM, whether an embedded DRAM array or a single-purpose DRAM
13 circuit. A capacitor according to the invention may be used in any circuit and is not
14 confined to a DRAM application.

15

16 Different materials may be used than those illustrated to perform the same functions.

17

18 The steps of the process may be continued to place another
19 dielectric/groundplate/dielectric/storage plate combination within the trench.

20

21 An example of a process sequence according to the invention may be summarized as
22 follows:

23

24 1 Form a deep trench

- 1 2 deposit a liner on the interior surface of the trench
- 2 2nm oxide, 4nm nitride, 10nm poly, 6nm nitride
- 3 3 Fill the trench with resist, recess the resist to 1.5um, strip the outer nitride layer
- 4 4 resist strip
- 5 5 oxidize the exposed poly in the upper portion.
- 6 6 strip the liner layers in the bottom, exposing the crystal silicon walls
- 7 7 trench bottle etch
- 8 8 optional HSG and HSG recess
- 9 9 gas phase doping for buried plate
- 10 10 first node nitride (re-ox)
- 11 11 first storage plate poly (optional HSG)
- 12 12 second node nitride (re-ox)
- 13 13 poly / nitride RIE to expose edge of first plate / buried plate
- 14 14 poly thermal oxide / expose buried plate
- 15 15 poly dep - second ground plate
- 16 16 resist / resist recess
- 17 17 poly RIE to clear upper portion
- 18 18 selective poly nitridation / re-ox
- 19 19 oxide wet etch - expose top edge of first storage plate
- 20 20 poly dep - second storage plate
- 21 21 collar formation, transistor formation, back end

22

23 Industrial Applicability

24

- 1 The invention applies to a method of forming a capacitor embedded in a substrate, such
2 as an integrated circuit substrate, that may be used in an electrical circuit, such as a
3 dynamic random access memory, and the structure of the capacitor formed by the method.
4 Capacitors formed according to the invention may be used in computers and other
5 electronic devices and systems.
6
7 While the invention has been described in terms of a single preferred embodiment, those
8 skilled in the art will recognize that the invention can be practiced in various versions
9 within the spirit and scope of the following claims.

What is claimed is:

- 1 1. A method of forming a capacitor in a substrate (10) comprising the steps of:
 - 2 etching a trench (60) in said substrate (10);
 - 3 forming a first capacitor plate (15) by diffusing a dopant into said substrate (10);
 - 4 depositing a first conformal dielectric layer (105) on an interior surface of said trench;
 - 5 depositing a first conductive storage plate (110) on an interior surface of said first
 - 6 dielectric layer (105);
 - 7 depositing a second conformal dielectric layer (115) on an interior surface of said first
 - 8 conductive storage plate (110);
 - 9 etching directionally through said second dielectric layer and said first storage plate to
 - 10 expose a substrate contact surface (16) of said first capacitor plate (15) whereby upper
 - 11 and lower edges (112) of said first storage plate are exposed;
 - 12 forming an insulator (122) covering said exposed upper and lower edges (112) of said
 - 13 first storage plate (110);
 - 14 depositing a second capacitor plate (120) on an interior surface of said second dielectric
 - 15 layer (115), to make electrical contact with said substrate contact surface (16);
 - 16 forming a third dielectric layer (125) on exposed interior surfaces of said second capacitor
 - 17 plate (120);
 - 18 removing said insulator covering said exposed upper edge of said first storage layer (122),
 - 19 thereby exposing said upper edge (112) of said first storage plate (110); and
 - 20 depositing a second conductive storage plate (130) abutting said third dielectric layer
 - 21 (125), thereby establishing electrical contact between said first (110) and second (130)
 - 22 conductive storage plates, which are separated from said first (15) and second (120)
 - 23 capacitor plates by said first (105), second (115) and third (125) dielectric layers.

- 1 2. A method according to claim 1, further comprising a step, before said step of
- 2 forming a first capacitor plate of, forming a dopant protective layer having an outer
- 3 nitride layer on the interior surface of said trench;
- 4 depositing resist, recessing said resist to a capacitor top position below a substrate
- 5 surface;
- 6 stripping said outer nitride layer above said capacitor top position;
- 7 stripping said dopant protective layer below said capacitor top position, thereby exposing
- 8 said substrate.

1

2 3. A method according to claim 2, in which said substrate is a silicon wafer;
3 said dopant protective layer comprises a layer of oxide adjacent to said substrate, a
4 layer of nitride, a layer of poly and an outer layer of nitride; and, after said step of
5 stripping said outer layer, further comprising a step of oxidizing said layer of poly.

- 1
2 4. A method according to claim 1, further comprising a step of performing a bottle
3 etch before said step of diffusing dopant into said substrate, thereby forming an upper
4 portion of said trench having a first width and a lower portion of said trench having a
5 second width greater than said first width.
6
7 5. A method according to claim 1, further comprising a step of forming a layer of
8 hemispherical grained silicon on an interior surface of at least one silicon layer.
9
10 6. A method according to claim 1, in which said step of forming a third dielectric
11 layer is performed by thermal nitridation.
12
13 7. A method according to claim 4, further comprising, after said step of forming said
14 first storage plate, a step of removing material from said first storage plate from said
15 upper portion of said trench, thereby forming a contact edge of said first storage plate.
16
17 8. A method according to claim 7, in which said second storage plate makes contact
18 with said first storage plate at said contact edge, disposed outside said first width of said
19 upper portion of said trench.
20
21 9. A method according to claim 1, further comprising a step of forming a transistor
22 having one electrode connected to said storage plate of said capacitor and a second
23 electrode connected to a cell electrode, thereby forming a DRAM cell.
24

1 10. A method according to claim 9, further comprising a step, before said step of
2 forming a first capacitor plate of, forming a dopant protective layer having an outer
3 nitride layer on the interior surface of said trench;
4 depositing resist, recessing said resist to a capacitor top position below a substrate
5 surface;
6 stripping said outer nitride layer above said capacitor top position;
7 stripping said dopant protective layer below said capacitor top position, thereby exposing
8 said substrate.

9
10 11. A method according to claim 10, in which said substrate is a silicon wafer;
11 said dopant protective layer comprises a layer of oxide adjacent to said substrate, a layer
12 of nitride, a layer of poly and an outer layer of nitride; and, after said step of stripping said
13 outer layer, further comprising a step of oxidizing said layer of poly.

14
15 12. A method according to claim 10, further comprising a step of performing a bottle
16 etch before said step of diffusing dopant into said substrate, thereby forming an upper
17 portion of said trench having a first width and a lower portion of said trench having a
18 second width greater than said first width.

19
20 13. A method according to claim 12, further comprising, after said step of forming
21 said first storage plate, a step of removing material from said first storage plate from said
22 upper portion of said trench, thereby forming a contact edge of said first storage plate.

23

24

1 14. A method according to claim 13, in which said second storage plate makes contact
2 with said first storage plate at said contact edge, disposed outside said first width of said
3 upper portion of said trench.

4
5 15. A capacitor formed in an integrated circuit substrate (10) comprising:
6 a trench (60) etched in said substrate;
7 a first capacitor plate (15) formed by diffusing a dopant into said substrate (10) outside
8 said trench (60);
9 a first conformal dielectric layer (105) deposited on an interior surface of said trench (60);
10 a first conductive storage plate (110) formed on an interior surface of said first dielectric
11 layer (105);
12 a second conformal dielectric layer (115) deposited on an interior surface of said first
13 conductive layer (110);
14 a second capacitor plate (120) deposited on an interior surface of said second dielectric
15 layer (115), said second capacitor plate (120) extending into the bottom of said trench
16 (60), passing through said second dielectric layer (115), said first storage plate (110) and
17 said first dielectric layer (105) and making electrical contact with said first capacitor plate
18 (15), said second capacitor plate (120) being isolated from said first storage plate (110);
19 a third dielectric layer (125) formed on exposed interior surfaces of said second capacitor
20 plate (120); and
21 a second conductive storage plate (130) deposited on an interior surface of said third
22 dielectric layer (125) and in electrical contact with said first conductive storage plate
23 (110) in an upper region of said trench above said second capacitor plate (120), said first
24 (110) and second (130) conductive storage plates being separated from said first (15) and

1 second (120) capacitor plates by said first (105), second (115) and third (125) dielectric
2 layers.

3
4 16. A capacitor according to claim 15, in which said trench has a lower portion
5 containing said first and second conductive storage plates and an upper portion
6 connecting said lower portion to a substrate surface, in which said upper portion has an
7 upper width and said lower portion has a lower width greater than said upper width.

8
9
10 17. A capacitor according to claim 16, in which said second storage plate makes
11 contact with said first storage plate at a contact edge disposed outside said first width of
12 said upper portion of said trench.

13
14 18. A capacitor according to claim 15, further comprising a transistor having one
15 electrode connected to said storage plate of said capacitor and a second electrode
16 connected to a cell electrode, thereby forming a DRAM cell.

17
18 19. A capacitor according to claim 18, in which said trench has a lower portion
19 containing said first and second conductive storage plates and an upper portion
20 connecting said lower portion to a substrate surface, in which said upper portion has an
21 upper width and said lower portion has a lower width greater than said upper width.

22
23 20. A capacitor according to claim 19, in which said second storage plate makes
24 contact with said first storage plate at a contact edge disposed outside said first width of

1 said upper portion of said trench.

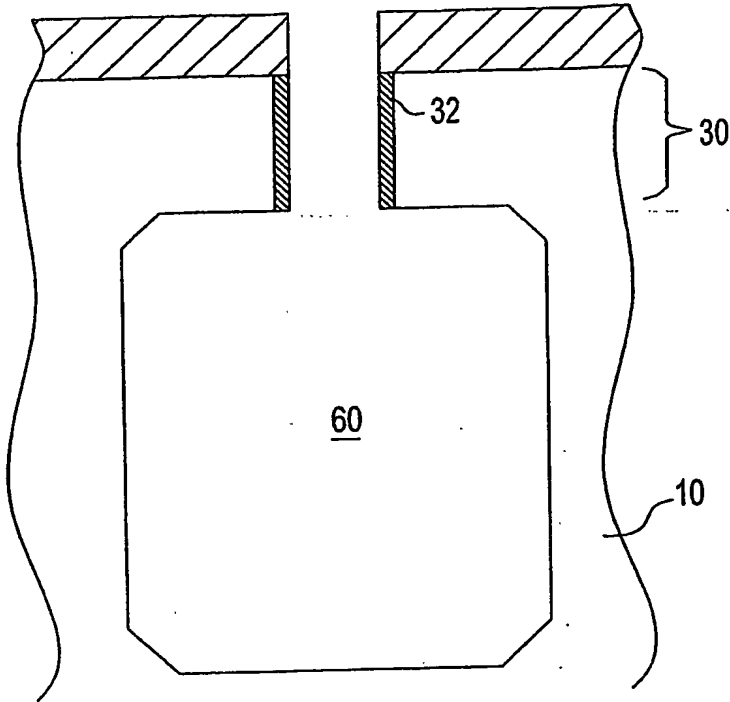


FIG. 1

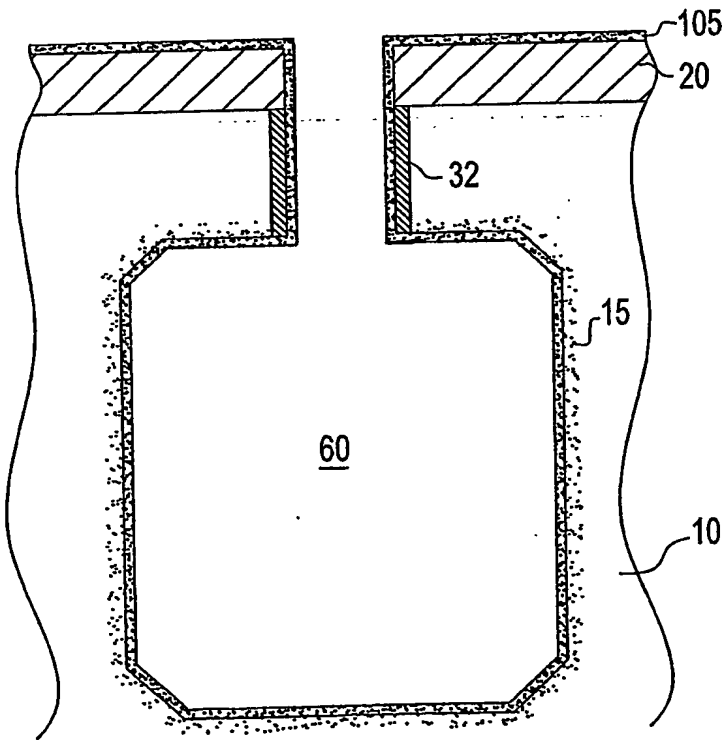


FIG. 2

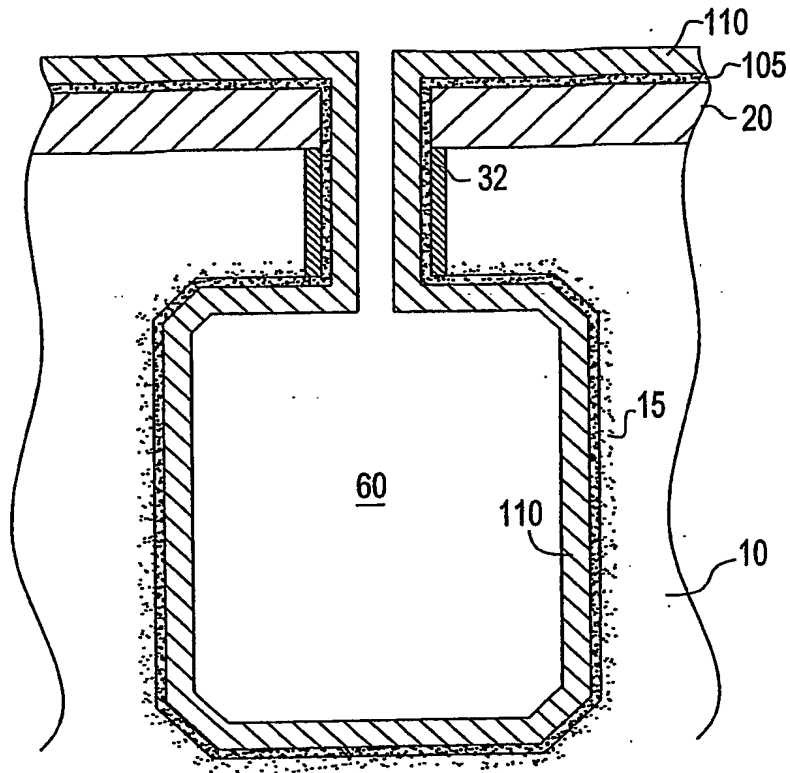


FIG. 3

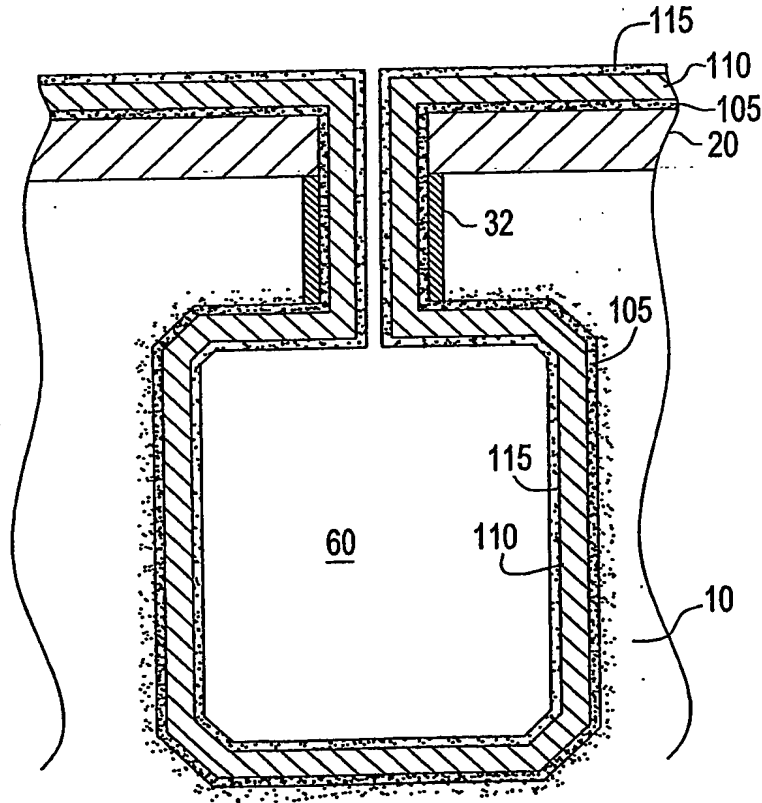


FIG. 4

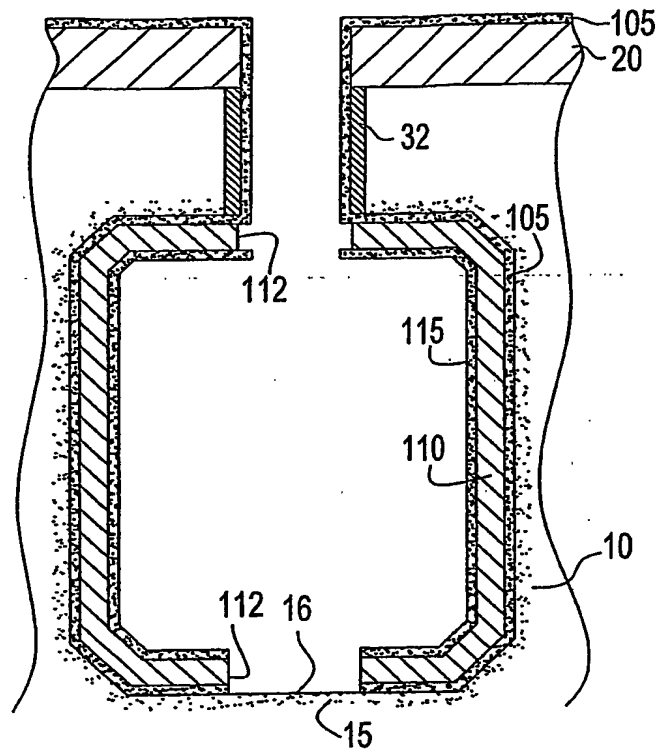


FIG. 5

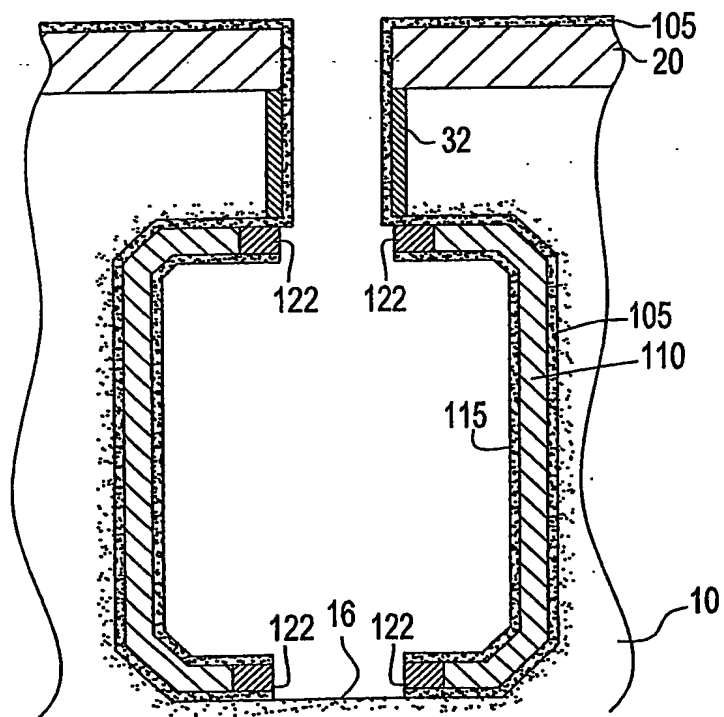


FIG. 6

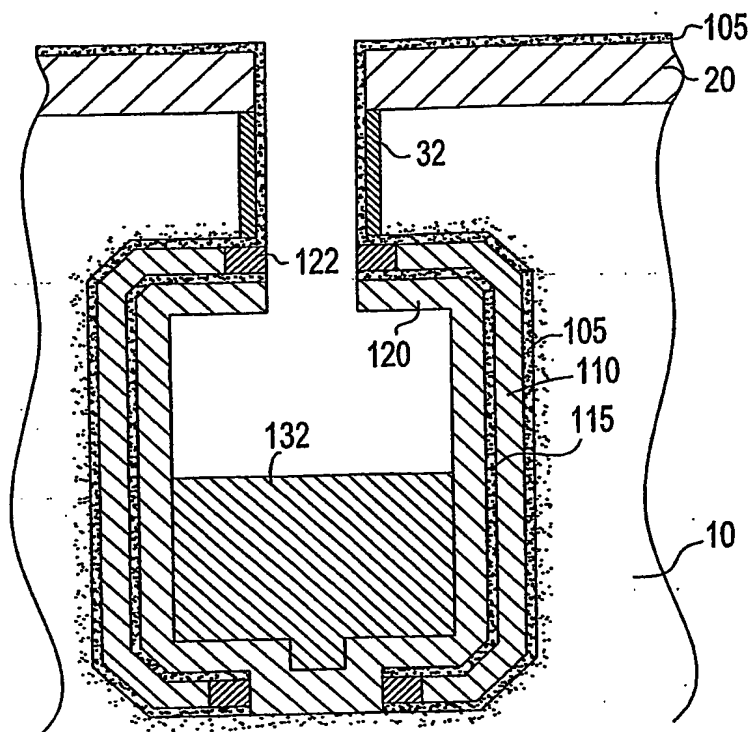


FIG. 7

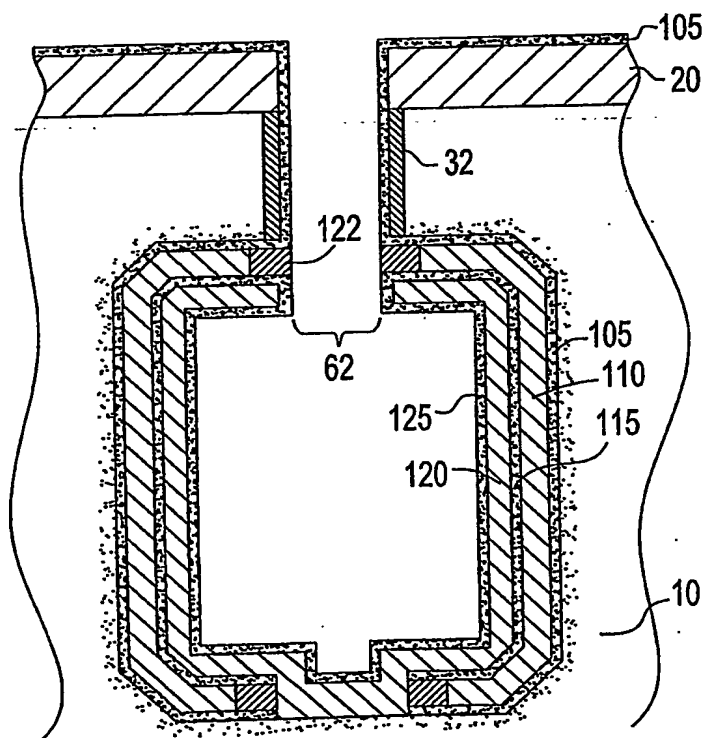


FIG. 8

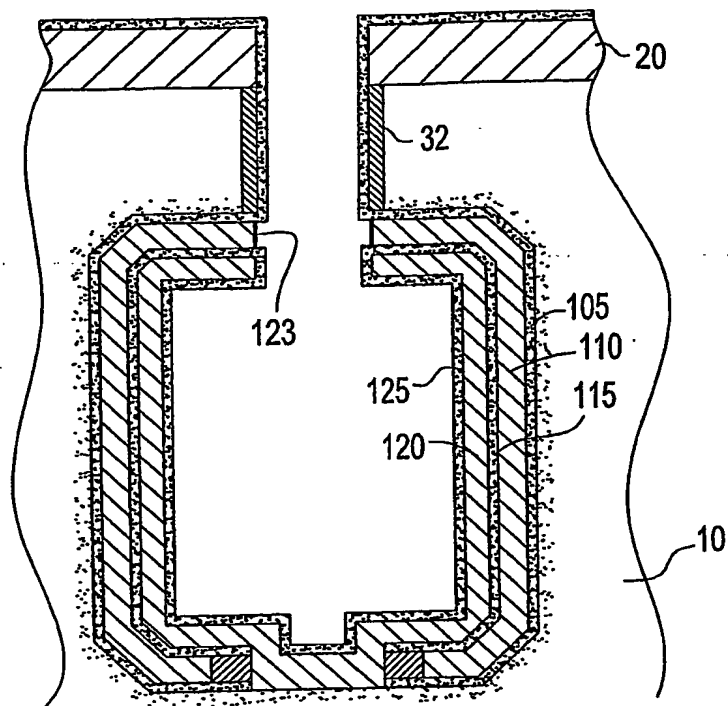


FIG. 9

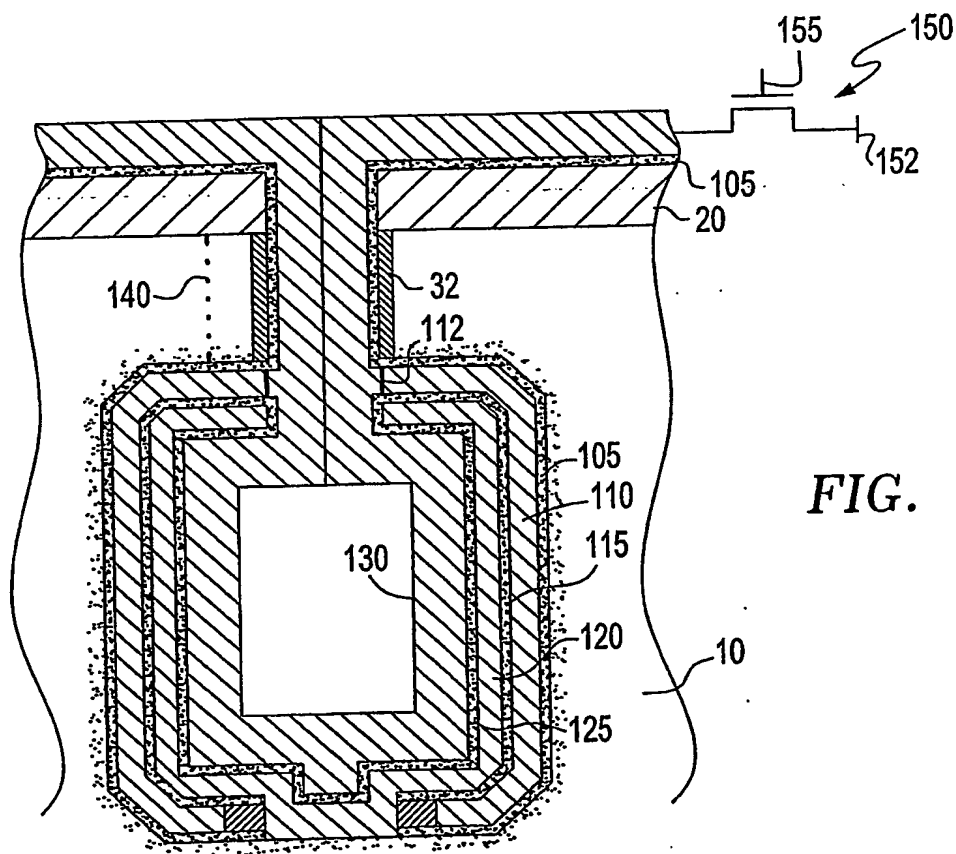


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US04/02648

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 21/8242

US CL : 438/243-249,386-392; 257/301-304

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/243-249,386-392; 257/301-304

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IBEE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
JPO, EPO, PGPUB, DERWENT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2003/0022457 A1 (Gutsche et al.) 30 Jan 2003 (30.01.2003), paragraphs [0033]-[0042].	1-20
Y	US 6150210 (Arnold) 21, Nov, 2000 (21.11.2000) column 5, line 61 to column 9, line 62.	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

20 July 2004 (20.07.2004)

Date of mailing of the international search report

30 NOV 2004

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